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IN THE CLAIMS:

1. (Currently amended) An emulation board, comprising:
a first integrated circuit, that is part of the emulation board, having a first
reconfigurable resource;
a first processing resource, that is part of the emulation board, in communication
with, and operable to configure, the first reconfigurable resource;
a first memory, that is part of the first processing resource, having stored therein
programmed instructions for configuring the first reconfigurable resource; and
a first processor, that is part of the first processing resource, for executing the
programmed instructions of the first memory.
~~An emulation logic board, comprising:~~
~~at least one integrated circuit having reconfigurable logic resources; and~~
~~on-board processing resources, in communication with the at least one~~
~~integrated circuit, operable to configure the integrated circuit.~~
2. (Currently amended) The emulation [logic] board of claim 1, further comprising
a plurality of integrated circuits, ~~each having~~reconfigurable [logic] resources that are
part of the emulation board, each reconfigurable resource having available at the on-
board processing resource[s], that is part of the emulation board, being operable to
configure each of the reconfigurable [logic] resource[s] of each of the integrated circuits.
3. (Currently amended) The emulation [logic] board of claim 1, wherein the first
reconfigurable resource~~integrated circuit further includes~~ is a reconfigurable input/output
resource. resources, the on-board processing resources being further operable to
configure the reconfigurable input/output resources.
4. (Currently amended) The emulation [logic] board of claim 1, wherein the first
reconfigurable resource is a reconfigurable logic resource, on-board processing

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~~resources comprise:~~

~~memory having stored therein programming instructions for configuring the
integrated circuit; and
a processor coupled to the memory to execute the programming instructions.~~

5. (Currently amended) The emulation [logic] board of claim 1, wherein the first reconfigurable resource is a further comprising reconfigurable interconnect[s] resource.
~~in communication with the integrated circuit and the on-board processing resources,
wherein the on-board processing resources are operative to configure the
reconfigurable interconnects.~~

6. (Currently amended) The emulation [logic] board of claim 1, wherein the first
~~on-board~~ processing resource[s] is[are] operable to configure the first reconfigurable
resource~~integrated circuit~~ in response to an external command[s].

7. (Currently amended) The emulation [logic] board of claim 6, wherein the
external command[s] comprises a data packet.

8. (Currently amended) The emulation [logic] board of claim 7, wherein the data
packet comprises:

a packet header;
a command field ~~following the packet header;~~ and
a parameter field ~~following the command field;~~ and
an end-of-packet marker following the parameter field.

9. (Currently amended) The emulation [logic] board of claim 1, wherein the first
integrated circuit comprises: ~~on-chip data processing resources operative to assist the
on-board processing resources to perform the configuration of the integrated circuit.~~
an on-chip processing resource, operative to assist the first processing resource
in configuring the first reconfigurable resource;

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an on-chip memory, that is part of the on-chip processing resource, having stored therein programmed instructions for configuring the first reconfigurable resource; and
an on-chip processor, that is part of the on-chip processing resource, for executing the programmed instructions of the on-chip memory.

10. (Currently amended) The emulation [logic] board of claim 1,
~~comprising: wherein the on-board processing resources are further operable to perform emulation functions on a configured integrated circuit.~~

a second reconfigurable resource that is part of the emulation board;
a second processing resource, that is part of the emulation board, in communication with, and operable to check a configuration of, the second reconfigurable resource;

a second memory, that is part of the second processing resource, having stored therein programmed instructions for confirming a configuration of the second reconfigurable resource; and

a second processor, that is part of the second processing resource, for executing the programmed instructions of the second memory.

11. (Currently amended) The emulation [logic] board of claim 10, wherein a confirmation is performed by comparing a configuration, of the second reconfigurable resource, to commands received.~~the emulation functions comprise generating testing stimuli and applying testing stimuli to an appropriate pin of the at least one integrated circuit.~~

12. (Currently amended) The emulation [logic] board of claim 1[10], further comprising:

a first software module, of the first memory, having programmed instructions for configuring the first reconfigurable resource; and

a second software module, of the first memory, that controls invocation of the first software module.

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~~where the emulation functions comprise:~~
~~locally determining emulation state elements of a design being emulated;~~
~~reading state data of the emulation state elements to detect occurrence of certain~~
~~events; and~~
~~reporting the occurrence of the events upon detection.~~

13. (Currently amended) The emulation [logic] board of claim 12, [10] wherein the second software module performs invocation of the first software module in on-board processing resources are operable to perform emulation functions response[ive] to an external command[s].

14. (Currently amended) In an emulation [logic] board comprising a first reconfigurable resource that is part of the emulation board, a first integrated circuit having at least part of the first reconfigurable resource, a first processing resource that is part of the emulation board, a first memory that is part of the first processing resource and a first processor that is part of the first processing resource, a method comprising:
receiving, by the first processing resource, a command to configure the emulation board;

executing programmed instructions, of the first memory by the first processor, for configuring the first reconfigurable resource; and

configuring, by the first processing resource, the first reconfigurable resource, at least one integrated circuit, having reconfigurable logic resources and on-board processing resources, in communication with the at least one integrated circuit, a method of configuring the emulation logic board comprising:

~~—receiving, by the on-board processing resources, a command for configuring the logic board; and~~

~~—configuring the emulation logic board in accordance with the command received by the on-board processing resources.~~

15. (Currently amended) The method of claim 14, wherein the first reconfigurable

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resource is a reconfigurable input/output resource.

~~configuring the emulation logic board in accordance with the external command comprises:~~

- ~~—— locally generating on the emulation logic board, by the on-board processing resources, a configuration signal to configure the at least one integrated circuit; and~~
- ~~—— applying the locally generated configuration signal to the integrated circuit.~~

16. (Currently amended) The method of claim 14, wherein the first reconfigurable resource is a reconfigurable logic resource.

~~emulation logic board further includes reconfigurable interconnects in communication with the integrated circuit and the on-board processing resources, and the on-board resources are operative to configure the reconfigurable interconnects, and wherein configuring the emulation board in accordance with the command comprises:~~

- ~~—— locally generating on the emulation logic board, by the on-board processing resources, a configuration signal to configure the at least one of the reconfigurable interconnects; and~~
- ~~—— applying the locally generated configuration signal to the at least one reconfigurable interconnect.~~

17. (Currently amended) The method of claim 14, wherein the first reconfigurable resource is a reconfigurable interconnect resource.

~~integrated circuit further comprises on-chip processing resources, configuring the integrated circuit is at least partially performed in conjunction with on-chip data processing resources.~~

18. (Currently amended) An emulation system comprising:
a computer having electronic design automation software to partition an integrated circuit design into a plurality of partitions;
a first emulation board external to, but in communication with, the computer;

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a first reconfigurable resource that is part of the first emulation board;
a first integrated circuit having at least part of the first reconfigurable resource;
a first processing resource that is part of the first emulation board, in
communication with, and operable to configure, the first reconfigurable resource in
response to commands from the electronic design automation software of the computer;
a first memory, that is part of the first processing resource, having stored therein
programmed instructions for configuring the first reconfigurable resource; and
a first processor, that is part of the first processing resource, for executing the
programmed instructions of the first memory.

~~a workstation having electronic design automation (EDA) software to partition an~~
~~integrated circuit (IC) design into a plurality of partitions; and~~
~~at least one emulation logic board in communication with the workstation,~~
~~comprising:~~

~~at least one integrated circuit having reconfigurable logic resources, and~~
~~on-board processing resources, in communication with the at least one~~
~~integrated circuit and operable to configure the integrated circuit in response to~~
~~commands from the EDA software of the workstation.~~

19. (Currently amended) The emulation system of claim 18, comprising: a
plurality of emulation logic boards.

a second emulation board external to the computer;
a second reconfigurable resource that is part of the second emulation board;
a second integrated circuit having at least part of the second reconfigurable
resource;
a second processing resource of the second emulation board, in communication
with, and operable to configure, the second reconfigurable resource in response to
commands from the electronic design automation software of the computer;
a second memory of the second emulation board, that is part of the second
processing resource, having stored therein programmed instructions for configuring the
second reconfigurable resource;

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a second processor of the second emulation board, that is part of the second processing resource, for executing the programmed instructions of the second memory; and

wherein the first and second emulation boards, that are external to each other, distributively configure the first and second reconfigurable resources.

20. (Currently amended) The emulation system of claim 19[18], further comprising:

a first software module, of the first memory, having the programmed instructions for configuring the first reconfigurable resource;

a third software module, of the first memory, that controls invocation of the first software module;

a second software module, of the second memory, having the programmed instructions for configuring the second reconfigurable resource; and

a fourth software module, of the second memory, that controls invocation of the second software module.

~~wherein the emulation logic board further comprises reconfigurable interconnects in communication with the integrated circuit and the on-board processing resources, wherein the on-board resources are operative to configure the reconfigurable interconnects.~~

21. (Currently amended) The emulation system as set forth in claim 18, wherein provision of programmed instructions by the computer, to the first memory, is staged, the on-board processing resources are further operable to perform emulation functions on a ~~configured integrated circuit in response to commands from the EDA software of the workstation.~~

22. (New) In an emulation system comprising a computer having electronic design automation software to partition an integrated circuit design into a plurality of partitions, a first emulation board external to the computer, a first reconfigurable

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resource that is part of the first emulation board, a first integrated circuit having at least part of the first reconfigurable resource, a first processing resource that is part of the first emulation board, a first memory that is part of the first processing resource and a first processor that is part of the first processing resource, a method comprising:

transmitting a first command from the electronic design automation software of the computer to the first processing resource;

executing programmed instructions, of the first memory by the first processor, for configuring the first reconfigurable resource; and

configuring, by the first processing resource, the first reconfigurable resource in accordance with the first command.

23. (New) The method of claim 22, where the emulation system further comprises a second emulation board external to the computer, a second reconfigurable resource that is part of the second emulation board, a second integrated circuit having at least part of the second reconfigurable resource, a second processing resource that is part of the second emulation board, a second memory that is part of the second processing resource and a second processor that is part of the second processing resource, the method further comprising:

transmitting a second command from the electronic design automation software of the computer to the second processing resource;

executing programmed instructions, of the second memory by the second processor, for configuring the second reconfigurable resource;

configuring, by the second processing resource, the second reconfigurable resource in accordance with the second command; and

wherein the first and second emulation boards, that are external to each other, distributively configure the first and second reconfigurable resources.

24. (New) The method of claim 23, further comprising the following steps:
executing programmed instructions, of a third software module of the first memory, that controls invocation of a first software module of the first memory;

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executing programmed instructions, of the first software module, for configuring the first reconfigurable resource;

executing programmed instructions, of a fourth software module of the second memory, that controls invocation of a second software module of the second memory; and

executing programmed instructions, of the second software module, for configuring the second reconfigurable resource;

25. (New) The method of 22, further comprising:
transferring, according to a staged process, programmed instructions from the computer to the first memory.

26. (New) The method of claim 14, wherein the command to configure is a data packet received from a system external to the emulation board.

27. (New) The method of claim 14, where the first integrated circuit further comprises an on-chip processing resource, an on-chip memory that is part of the on-chip processing resource and an on-chip processor that is part of the on-chip processing resource, the method further comprising the following steps:

executing programmed instructions, of the on-chip memory by the on-chip processor, for configuring the first reconfigurable resource; and

configuring, by assistance of the on-chip processing resource, the first reconfigurable resource.

28. (New) The method of claim 14, where the emulation board comprises a second reconfigurable resource that is part of the emulation board, a second processing resource that is part of the emulation board, a second memory that is part of the second processing resource and a second processor that is part of the second processing resource, the method further comprising the following steps:

executing programmed instructions, of the second memory by the second

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processor, for confirming a configuration of the second reconfigurable resource; and
checking with the second processing resource, that is in communication with the
second reconfigurable resource, a configuration of the second reconfigurable resource.

29. (New) The method of claim 14, further comprising the following steps:
executing programmed instructions, of a second software module of the first
memory, that control invocation of a first software module of the first memory; and
executing programmed instructions, of the first software module, for configuring
the first reconfigurable resource.